

# Key Enabling Materials for 3D-IC Fabrication and Device Performance

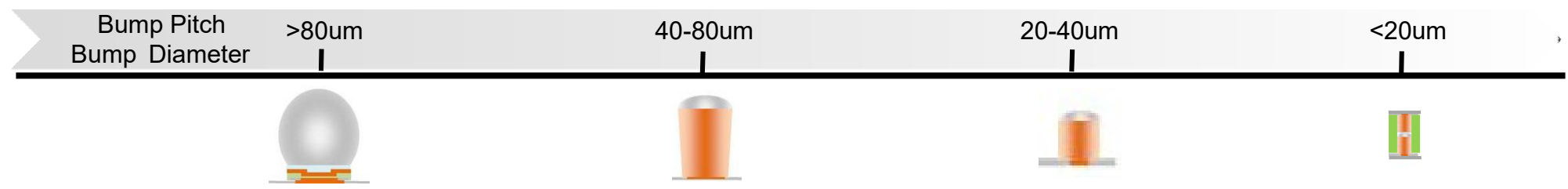
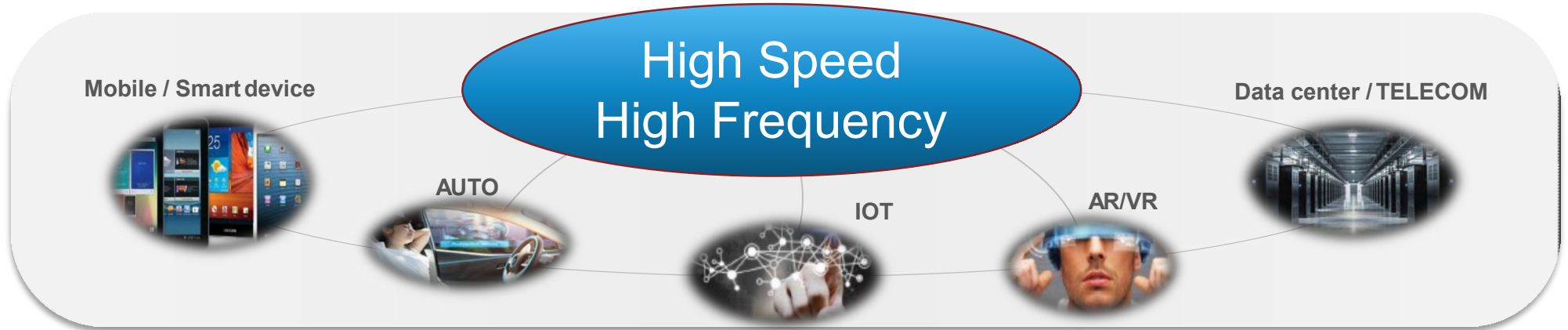
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DuPont Electronics and Imaging – Semiconductor

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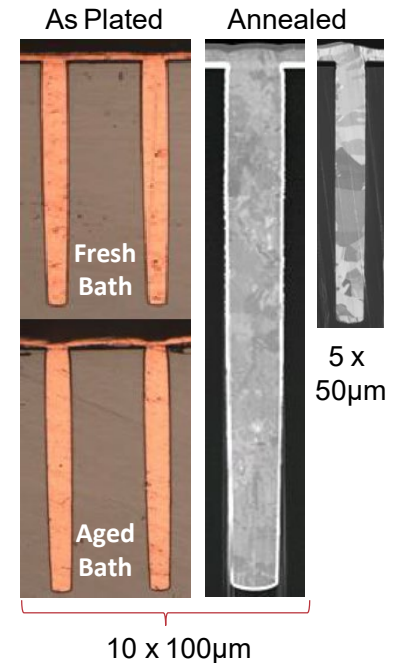


# Global Market Trend for Devices and Packaging



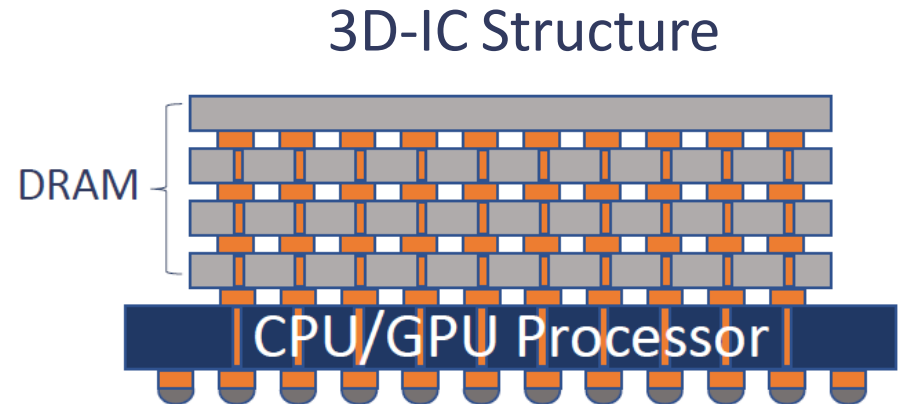
# Key Challenges to Enabling 3D-IC and Hybrid Bonding

- TSV formation (Via Middle)
  - Photoresists with good resolution and superior etch selectivity
  - Cu plating with fast plating rate, minimal overburden, and long bathlife
- Copper pillar and RDL plating
  - Chemical stability of photoresists to plating baths and pattern resolution,
  - EP Cu pillar with copper purity, crystallite size and grain orientation
- **Polymer adhesive layer**
  - Planar coating and polymer reflow over topography
  - Rheology modified after soft cure: non-tacky at RT forCMP and good flow at bonding temperature
  - Controlled removal rate of both polymer and copper
- Hybrid Bonding process
  - Low temperature for Cu-Cu joining and polymer bonding
  - No reaction of polymer with gas phase (formic acid) and liquid no residue fluxing agents
  - Use conventional Flip Chip bonding processes



# Achieving Reliable 3D-IC and Cu-Cu Hybrid Bonding

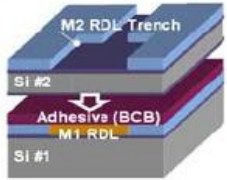
- Micro Electro-Mechanical & Micro Optical devices are currently the two most important applications driving permanent bonding applications.
- 3D-IC will be the driver for market growth in permanent bonding as designers continues to shrink devices to improve performance.
- 3D-IC Bonding Requirements
  - Controlled Rheology and Thermal Stability
  - Alignment Accuracy and ToolThroughput
  - Planar Surfaces and Copper-Copper Bonding
  - High Yield / Lower CoO
- Bonding Approaches
  - Anodic / Si Direct / Eutectic / **Adhesive /Hybrid**
- Adhesive Bonding Advantages
  - Low Bonding Temperature / High Bond Strength
  - CMP Planarization / Adhesive Reflow / Lower CoO



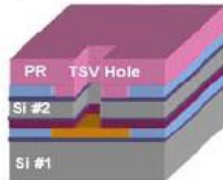
# Proposed Integration Schemes for C2C / C2W / W2W Bonding

## Via Last Process: WoW Consortium IITC 2012

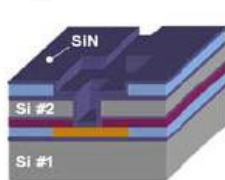
1) Wafer level bonding



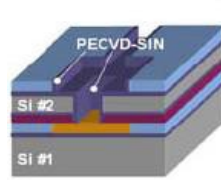
2) TSV PR & Si DRIE



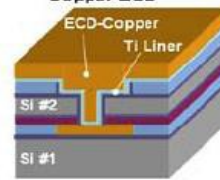
3) PECVD



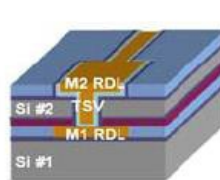
4) SiN Self-align Etching



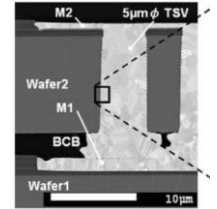
5) PVD metal barrier & Copper ECD



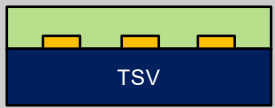
6) Planarization



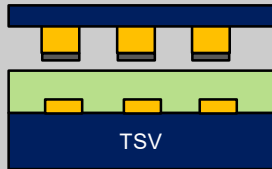
5µm TSV



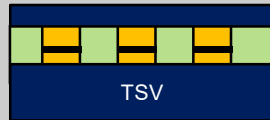
## NCP/NCF Process



1) Coating

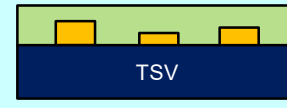


2) Alignment



3) Bonding

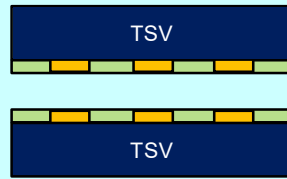
## Hybrid Bonding Cu-Cu or Cu-Sn and Polymer Adhesive



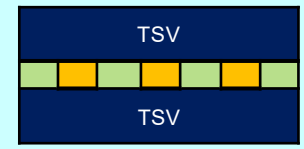
1) Coating



2) CMP Planarization

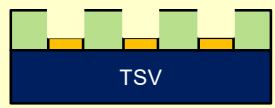


3) Alignment & Flux

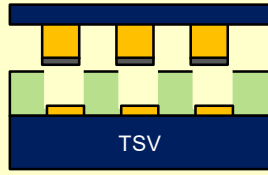


4) Bonding

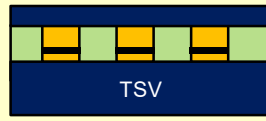
## Photo Patterned



1) Photopattern Dielectric



2) Plasma Clean

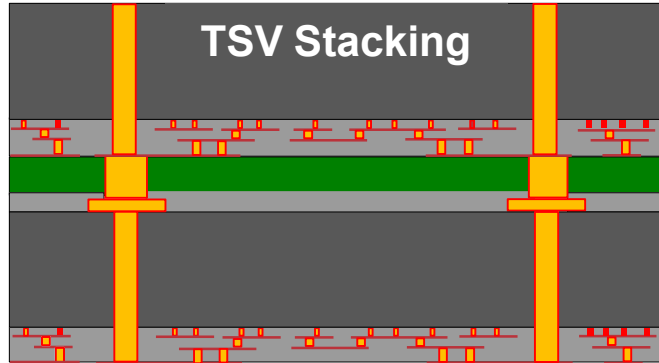


3) Align and Bond

# DuPont E&I Materials that Enable 3D-IC and Hybrid Bonding

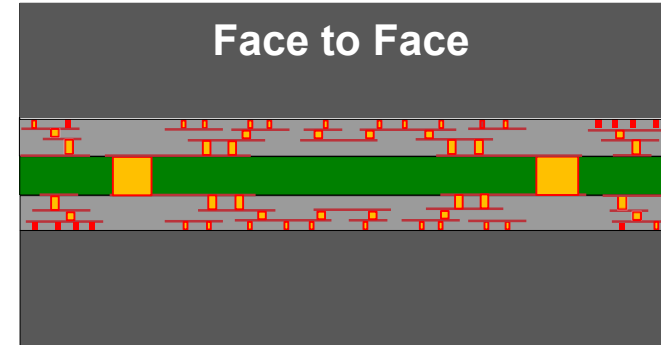
## CMP Consumables

- CMP Pads
- Copper Selective Slurries
- Dielectric Slurries
- CMP Cleaning Solutions



## Copper Plating

- Cu TSV Plating
- Cu RDLC and Pillar Plating
- Sn/Ag, Pure Sn and In Plating
- ENIG and EP Ni Barrier



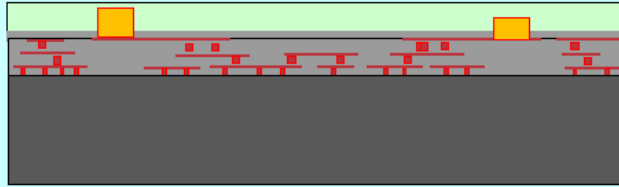
## Plating Photoresists

- Spin-on Photoresists
- Dry Film Photoresists
- Chem Amp i-Line

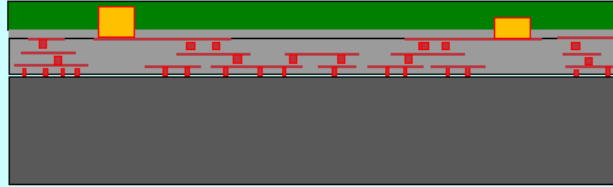
## Dielectric Materials

- Polymer Adhesives
- Spin-on Photodielectric
- Dry Film Photodielectrics
- Adhesion Promoters

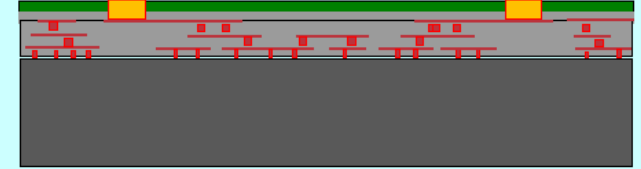
# 3D-IC Hybrid Bonding – Integration Process Flow



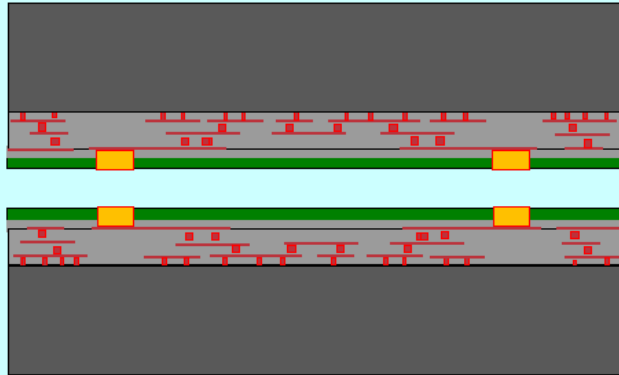
1. Deposit Polymer Adhesive



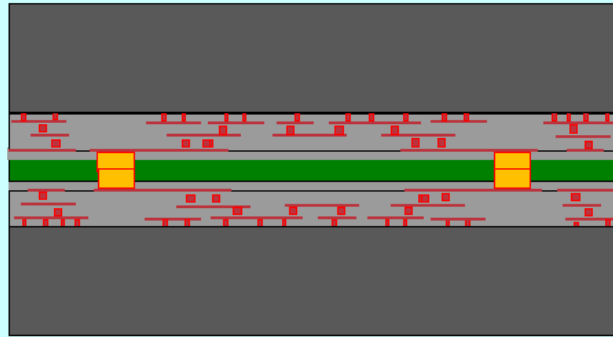
2. Soft Cure Polymer Dielectric



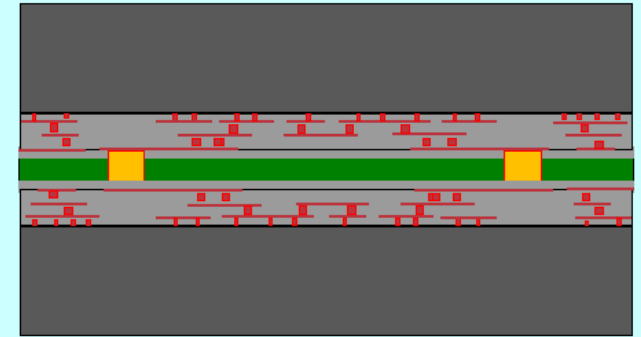
3. CMP Polymer + Cu pillar



4. Flux and Align Die



5. TCB Bond Die – Polymer Bonding

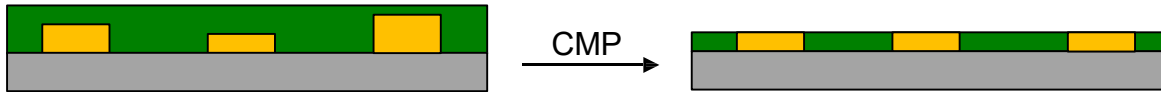


6. Copper Anneal

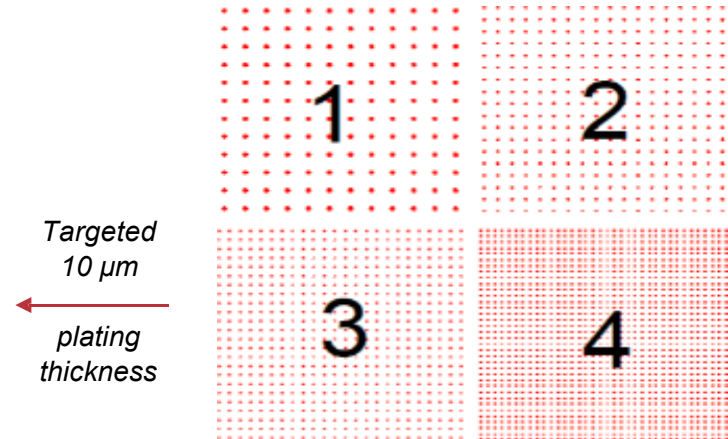
# Uniformity Critical for Hybrid Bonding



- Very good WID uniformity for pillar height is obtained for each die type with range of 0.3 $\mu$ m or 1.4% total height.
- While range in pillar height was quite low, it is still too large for successful Cu-Cu joining
- *CMP is required to achieve the desired height variance for Cu-Cu joining and polymer bonding*



IMAT BTP1C(200mm)	Quadrant			
Quadrant	1	2	3	4
Bump diameter ( $\mu$ m)	150	100	75	50
Pitch ( $\mu$ m)	600	400	300	200
Bump array (200mm)	12x12	18x18	24x34	36x36
Placement	Lattice	Lattice	Lattice	Lattice
Bump area (%)	4.5%	4.5%	4.5%	4.5%
Avg Cu Pillar Ht ( $\mu$ m)	10.0	10.0	9.8	9.6
Range ( $\mu$ m)	0.3	0.3	0.3	0.3
WID Uniformity	1.4%	1.4%	1.4%	1.5%
<i>Copper pillar plating was performed in Cheonan Applications Lab</i>				





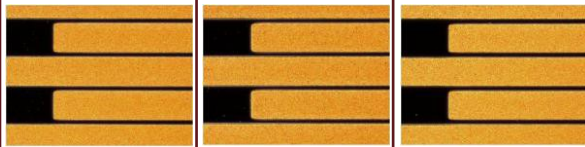
# Critical Properties for Polymer Dielectrics



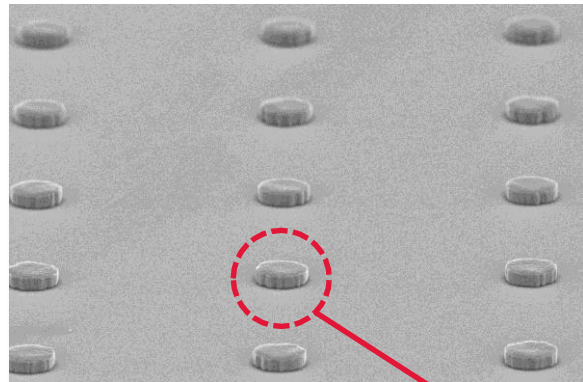
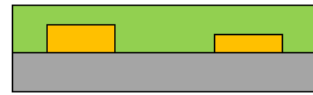
- Good planarization and reflow for coating
- Controllable rheology for CMP using soft cure
- Thermal stability of 350°C stable to PE-CVD
- No outgassing during cure, <1%wt loss/hr at 300°C
- Low dielectric constant, 2.55,  $\tan \delta$ , 0.0014 @ 40GHz
- Low water uptake, <0.2% @ 20°C/85%RH
- Low Cu migration, <10<sup>8</sup> ions/cm<sup>2</sup> @200°C
- Stable to gas phase (formic acid) fluxing
- Compatible with Au:Cu and Cu:Cu fusion processes

## Copper Electromigration

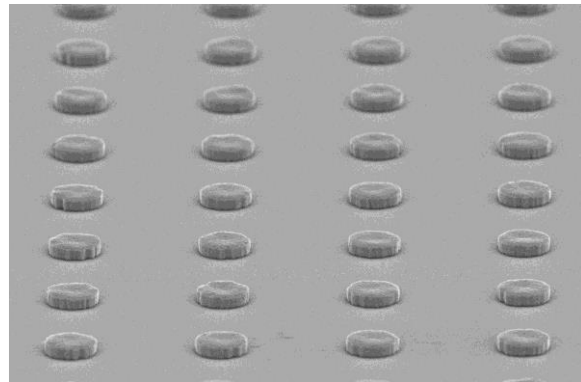
Biased HAST 130°C/85%RH	Bias V	Resistance ohm	
		Initial	After HAST
Polymer Dielectric	3	>1E+12	>1E+12
	5	>1E+12	>1E+12
	15	>1E+12	>1E+12



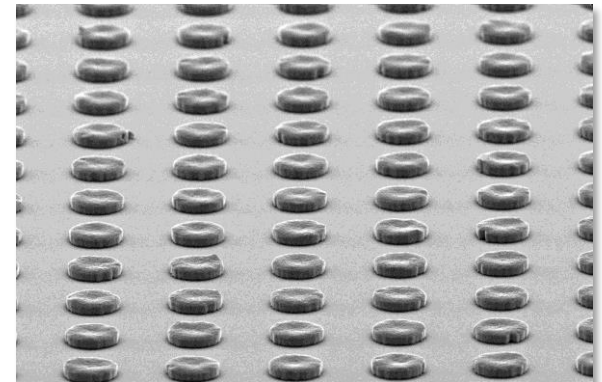
# Planar Coating of Polymer Dielectric over Copper Pillars



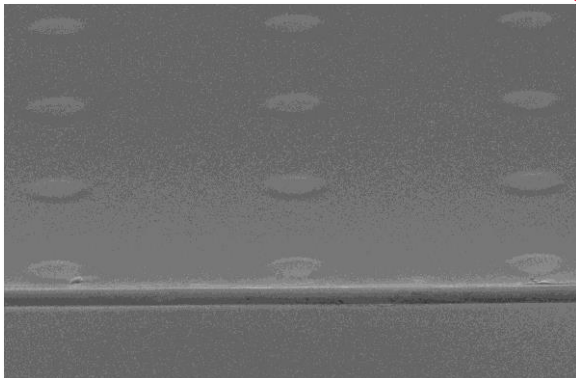
1:4



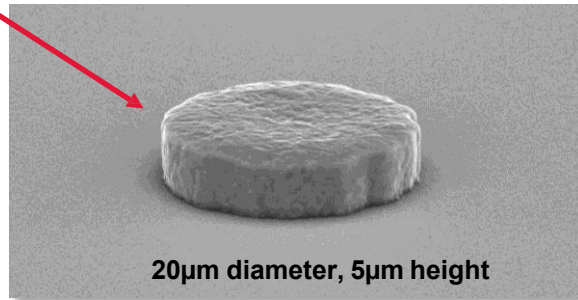
20µm diameter Cu pillar with different pitches



1:1

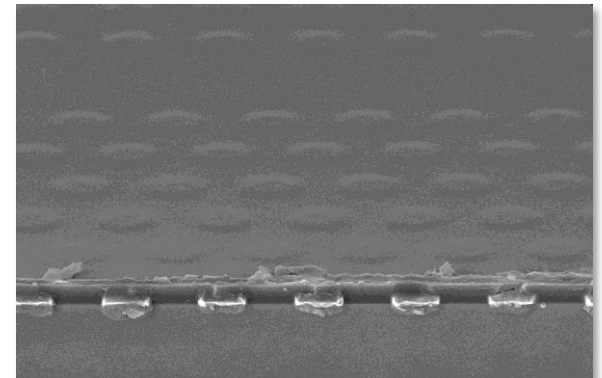


Polymer on less dense Cu Pillar



20µm diameter, 5µm height

Excellent conforming on Cu Pillar

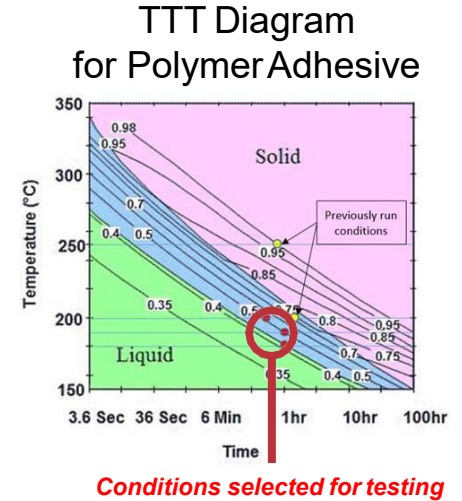
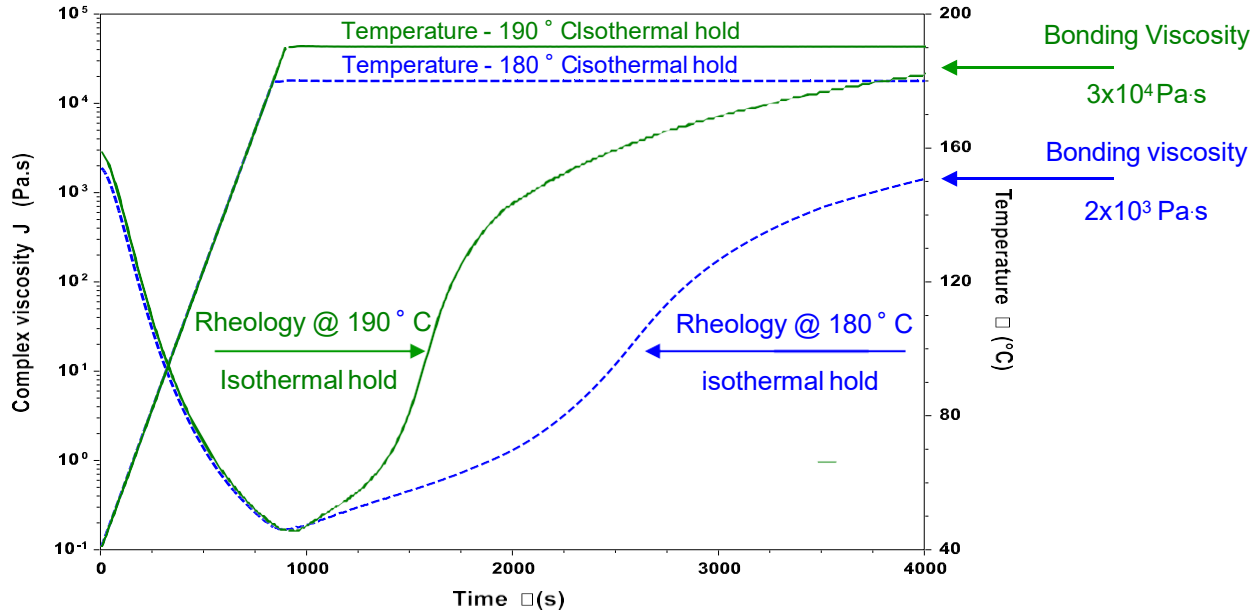


Polymer on dense Cu Pillar

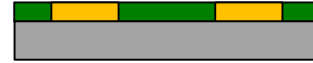
# Adjusting Hardness while Maintaining Flow Enables CMP



- Low viscosity polymer adhesive allows good coating uniformity and planarization over topography
- Soft curing (B-staging) polymer adhesive increases the modulus and hardness at RT to allow CMP
- Partial cured polymer dielectric has viscosity at bonding of  $10^3$  -  $10^5$  Pa·s



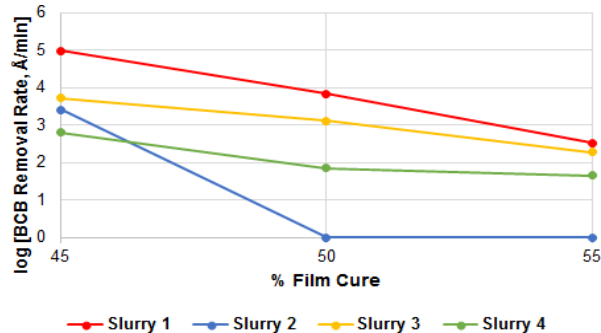
# Removal Rate of Polymer Dielectric Controlled by Soft Cure



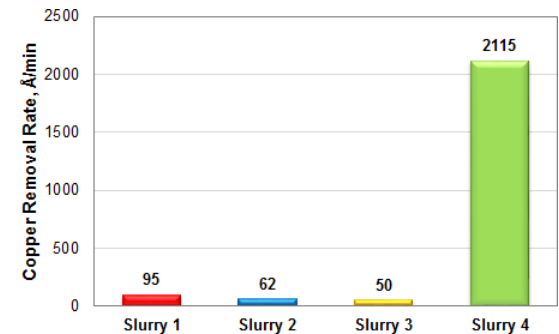
Formulation	Material Removal Rate, Å/min			
	Polymer Dielectric			Copper
Soft Cure Condition	<b>180°C/60min</b>	<b>190°C/60min</b>	<b>200°C/45min</b>	—
Degree of Cure	45%	50%	55%	
Viscosity at Temperature	2x10 <sup>3</sup> @ 180°C	3x10 <sup>4</sup> @ 190°C	>10 <sup>5</sup> @ 200°C	
Slurry 1	97580	6788	335	95
Slurry 2	2575	1	1	62
Slurry 3	5166	1283	192	50
Cu Slurry 4	637	72	45	2115

Strasbaugh 6EC 200 mm R&D polisher; IC1010™ pad; 2 psi; 93/87 rpm table/carrier speeds; 200 mL/min slurry flow; Saesol 8031C1 disk, 7 lbf

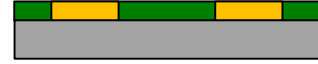
- Removal rate is controlled by both CMP processing conditions and soft cure temperature



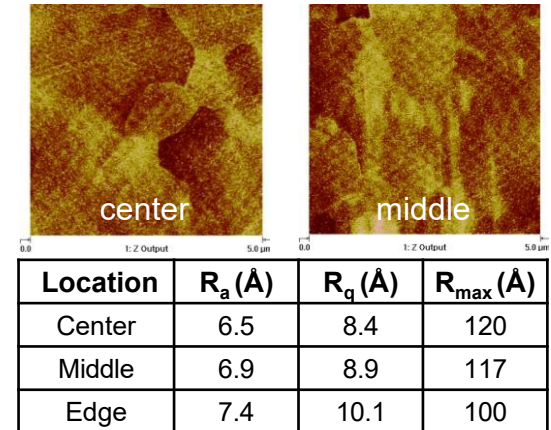
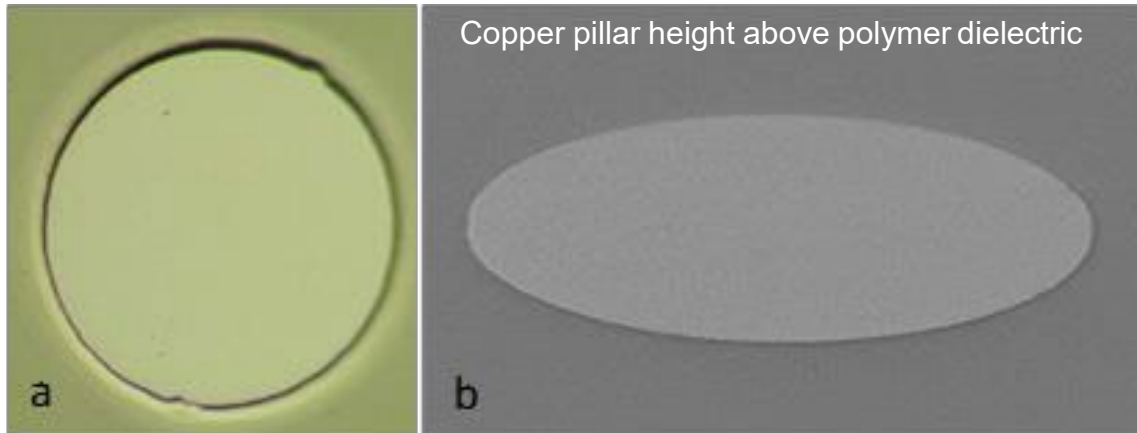
Non-selective copper and polymer removal process is under development



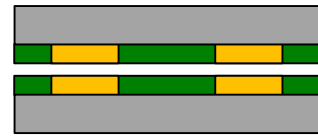
# Optimization of CMP Required for 3D-IC Hybrid Bonding



- Process adjustments and slurry design facilitated controlled polymer dielectric and copper removal on blanket films and in copper pillar/polymer structured wafers
- Excellent uniformity across the wafer and across copper pillars can be achieved
- Due to thermal expansion mismatch between Cu and polymer, Cu pillar is left exposed by ~10-20 nm
- A **strong collaboration between CMP and APT businesses** enabled material, formulation and process tuning to achieve topography control of patterned copper pillar/polymer structures

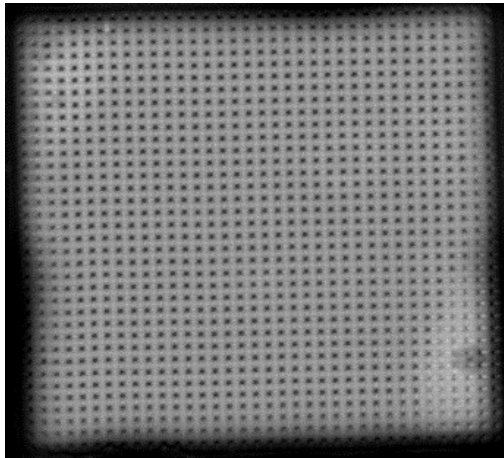
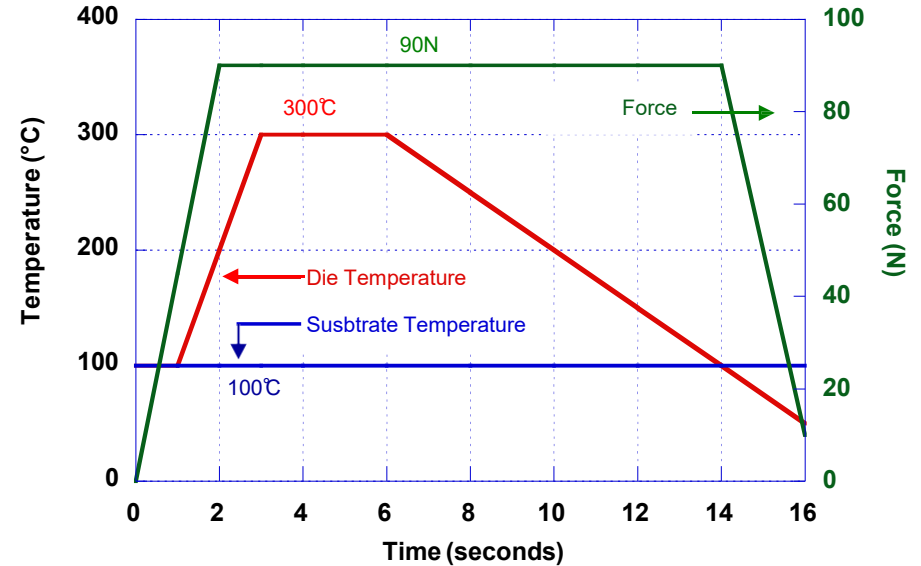


# TCB Bonding Process Used to Achieve Cu-Cu Joining



Typical TCB Process: *Toray FC3000S*

- Bring die in contact Cu-Cu only 90N force @ 100°C
- Ramp top die from 100°C→300°C 90N in 2 sec
- **Hold top die at 300°C / 90N for 4 sec**
- Cool top die to 100°C / 10N
- Release bond head

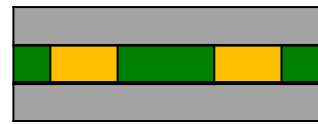


*Good Cu-Cu joining (dark areas)*

*No voiding seen in the field area*

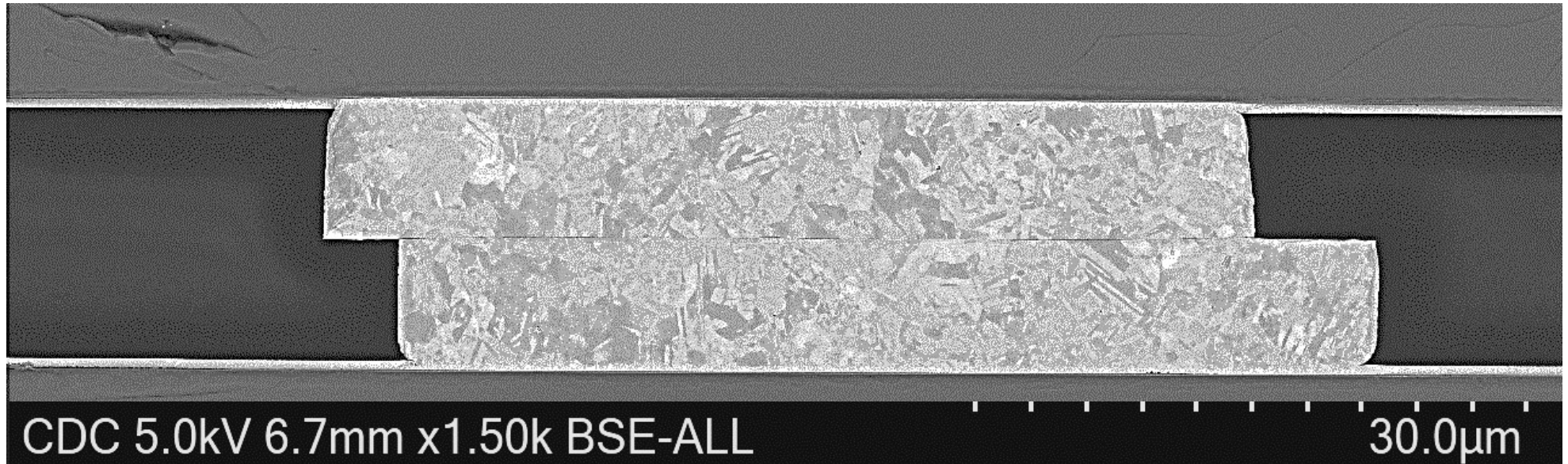
*CSAM - 100 MHz transducer*

# Cu-Cu Joining and Polymer Bonding Results

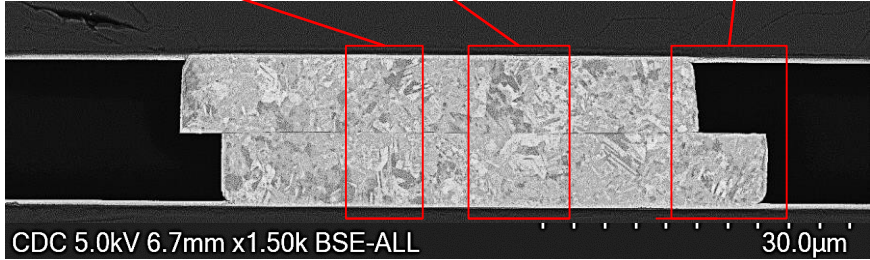
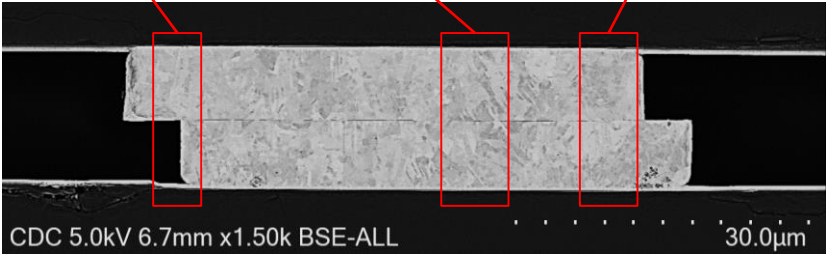
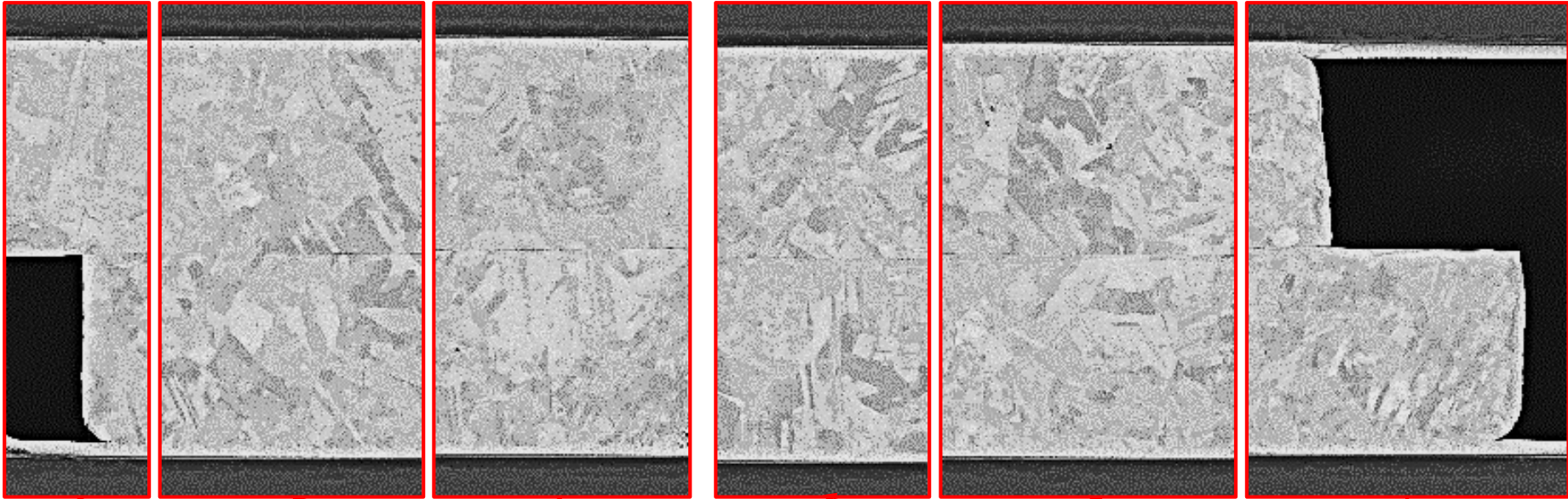
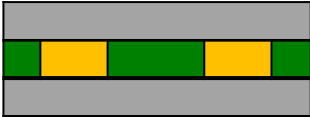


## Join/Bond processing improvements

- Cu–Cu Joining observed and good Polymer Dielectric bonding with no voiding
- Gas phase fluxing will remove copper oxide without impacting polymer bonding
- TCB process optimization will focus on temperature and pressure profile

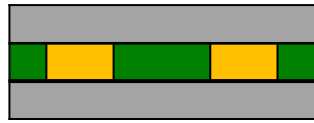


# Achieving Copper-Copper Joining and Polymer Bonding





# Summary of Current Work

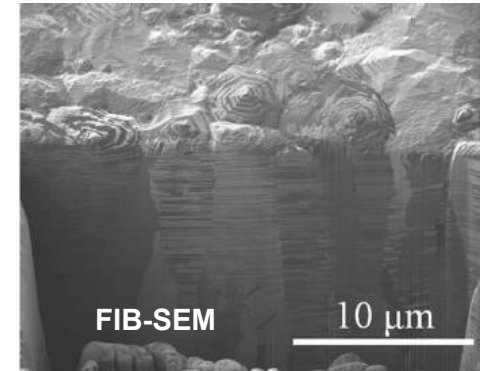


- ✓ Copper pillar plating delivers pillar of uniform height with high purity and small crystallite size
- ✓ Polymer dielectrics provide planar coatings and the controllable rheology for both CMP and bonding
- ✓ CMP slurry selection and process variables allow planarization of both Cu and polymer dielectric
- ✓ Cu-Cu joining demonstrated using a TCB bond tool using 90N of force and <4 sec bond time
- ✓ Low temperature bonding conditions were used, 300°C on the top die and 100°C on the bottom die
  
- ✓ Successful hybrid bonding results were demonstrated using polymer resin, copper grain structure and selective CMP processes developed across **DuPont Electronics & Imaging** business portfolio.
- ✓ This will enable broader and faster adoption of 3D-IC technology

# Plating Cu with Higher Diffusion for Low Temp. Joining



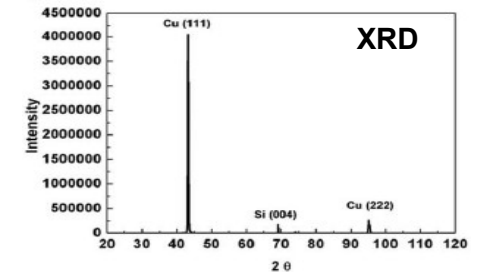
- Lower temperature processing required for DRAM and advanced node devices to minimize damage
- Surface diffusion of Cu ions across bonding interface is essential for reliable join
- Copper (111) can be plated with commercial EP Cu chemistry
- Different orientations of Cu provide widely different Cu diffusion rates:
- Cu (111) also has lowest Cu oxidation rate of all planes



Temperature	Cu (111)	Cu (100)	Cu (110)
150°C	$6.85 \times 10^{-6}$	$2.15 \times 10^{-10}$	$6.61 \times 10^{-12}$
200°C	$9.42 \times 10^{-6}$	$1.19 \times 10^{-9}$	$5.98 \times 10^{-11}$
250°C	$1.22 \times 10^{-5}$	$4.74 \times 10^{-9}$	$3.56 \times 10^{-10}$
300°C	$1.51 \times 10^{-5}$	$1.48 \times 10^{-8}$	$1.55 \times 10^{-9}$

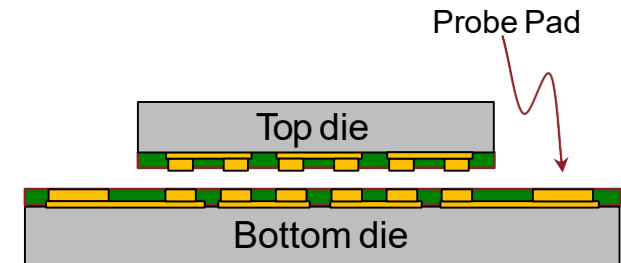
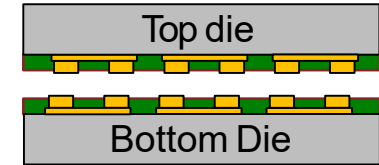
Liu et. al., Scientific Reports, 2015

Surface Diffusivity,  $D$  ( $\text{cm}^2/\text{sec}$ )



# Next Steps for 3D-IC Cu-Cu Joining and Polymer Bonding

- Copper pillar structures featuring sub 20 micron pillars at 1:1 pitch
  - Segment plate copper pillars, e.g. Cu(111)
  - Coat polymer adhesives, e.g. low temp cure
  - CMP segments using different process conditions
  - Dice segments and TCB bond
  - Reliability testing and failure analysis
  
- Via chain structure featuring sub 20 micron pillars and pads at 1:1 pitch
  - Repeat DOE with electrically testable segments
  - Validate bonding based on resistance measurement
  - Reliability testing and failure analysis



# Thank You



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